Amendments to the Claims :

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (original) An apparatus for continuous phase quadrature amplitude modulation and demodulation, the apparatus comprising:

a continuous phase quadrature modulator having a first multiplier multiplying an I-channel by a cosine wave weighted function, a second multiplier multiplying an output signal of the first multiplier by a cosine wave of a carrier frequency, a delay delaying a Q-channel by a predetermined time, a third multiplier multiplying the Q-channel by a sine wave weighted function, a fourth multiplier multiplying an output signal of the third multiplier by the sine wave of the carrier frequency, and an adder adding an output signal of the second multiplier and an output signal of the fourth multiplier; and

a continuous phase quadrature demodulator having a fifth multiplier multiplying the I-channel by the cosine wave of the carrier frequency, a sixth multiplier multiplying a signal from the fifth multiplier by the cosine wave weighted function, a first integrator and sampler integrating a signal from the sixth multiplier for the symbol duration time, a seventh multiplier multiplying the Q-channel by the sine wave of the carrier frequency, an eighth multiplier multiplying a signal from the seventh multiplier by the sine wave weighted function, and a second integrator and sampler integrating a signal from the eighth multiplier by the symbol duration time.

2. (original) The apparatus of claim 1, further comprising a signal mapper that separates a received binary data to the I-channel and the Q-channel and outputs the I-channel and the Q-channel to the first multiplier and the delay, respectively.

3. (original) The apparatus of claim 1, further comprising a first oscillator that outputs the cosine wave weighted function.

4. (original) The apparatus of claim 3, further comprising a first phase shifter that phase-shifts the cosine wave weighted function output from the first oscillator by 90 degrees and outputs the sine wave weighted function.

5. (original) The apparatus of claim 1, wherein the cosine wave weighted function is $\cos w_i t$.

6. (original) The apparatus of claim 1, wherein the cosine wave of the carrier frequency is $\cos w_c t$.

7. (original) The apparatus of claim 1, wherein the predetermined time is the half of a symbol duration time.

8. (original) The apparatus of claim 1, further comprising a second oscillator that outputs the cosine wave of the carrier frequency.

9. (original) The apparatus of claim 8, further comprising a second phase shifter that phase-shifts the cosine wave of the carrier frequency output from the second oscillator by 90 degrees and outputs the sine wave of the carrier frequency.

10. (original) The apparatus of claim 1, wherein the sine wave weighted function is $\sin w_i t$.

11. (original) The apparatus of claim 1, wherein the sine wave of the carrier frequency is $\sin w_c t$.

12. (original) The apparatus of claim 1, further comprising a phase locked loop (PLL) that controls the phase of a received signal.

13. (original) The apparatus of claim 12, further comprising a clock generator that receives a signal from the PLL and generates a clock cycle having a predetermined amount of time.

14. (original) The apparatus of claim 12, further comprising a third phase shifter that phase-shifts the cosine wave of the carrier frequency transferred from the PLL by 90 degrees and generates the sine wave of the carrier frequency.

15. (original) The apparatus of claim 13, further comprising a second oscillator that receives the clock cycle from the clock generator and outputs the cosine wave weighted function.

16. (original) The apparatus of claim 15, further comprising a fourth phase shifter that phase-shifts the cosine wave weighted function from the second oscillator by 90 degrees and outputs the sine wave weighted function.

17. (original) The apparatus of claim 1, further comprising a first determiner that determines an integral signal from the first integrator and sampler.

18. (original) The apparatus of claim 1, further comprising a second determiner that determines an integral signal from the second integrator and sampler.

19. (currently amended) The apparatus of claim 17 ~~or 18~~, further comprising a signal demapper that receives signals from the first determiner and the second determiner and outputs a binary data.